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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/668,454	09/22/2003	Ta-Chung Wu	17620R-002600US	2352

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EXAMINER

NGUYEN, KHIEM D

ART UNIT

PAPER NUMBER

2823

DATE MAILED: 04/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/668,454

Applicant(s)

WU ET AL.

Examiner

Khiem D. Nguyen

Art Unit

2823

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 02 February 2005.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-25 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-25 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 22 September 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on February 02nd, 2005 has been entered. A new rejection is made as set forth in this Office Action. Claims (1-25) are pending in the application.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Beintner et al. (U.S. Patent 6,566,228).

In re claim 1, **Beintner** discloses a method of forming a bottom oxide layer in a trench structure, the method comprising:

(a) providing a semiconductor substrate **10** and forming a trench structure **15a'** on the semiconductor substrate **10** (col. 7, lines 29-38 and FIG. 30);

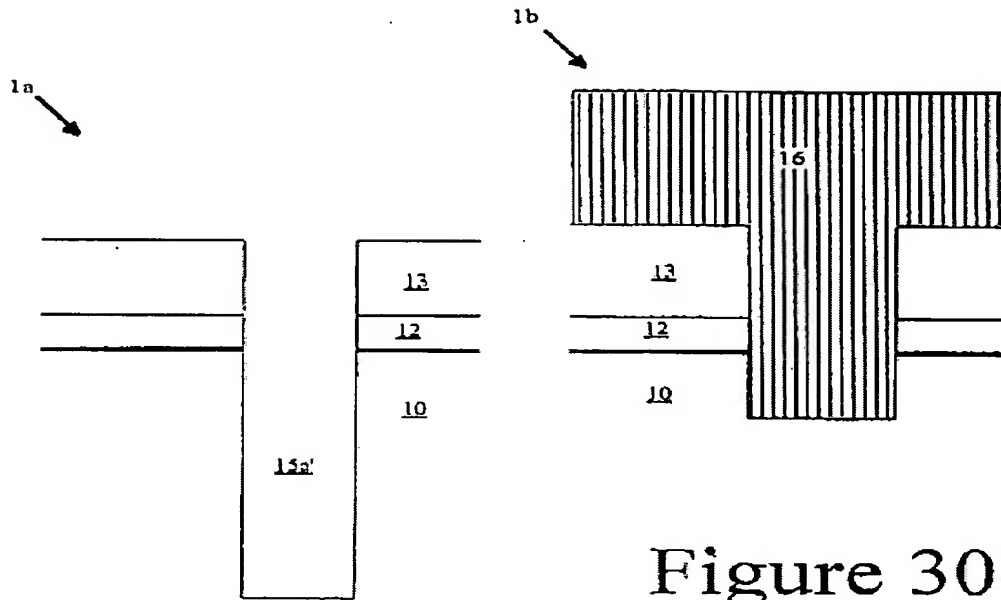


Figure 30

(b) performing a the plasma-enhanced chemical vapor deposition (PECVD) process without bias sputtering with tetraethylorthosilicate (TEOS) as a gas source at a temperature of about 440°C to about 520°C to deposit an oxide layer **22** on the bottom and sidewall of the trench structure **15a'** and the semiconductor substrate **10**, the oxide layer **22** only partially filling the trench **15a'** (col. 8, lines 52-60 and FIG. 32); and

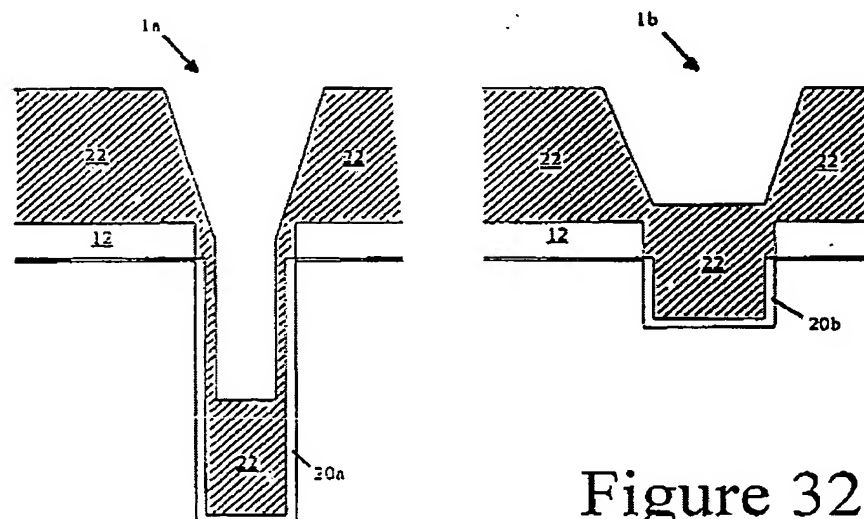


Figure 32

(c) removing, using a single etching process, the oxide layer **22** on the sidewall of the trench structure “substantially” completely and the oxide layer **22** on the bottom of the trench structure partially to define a remaining oxide layer **22'** as the bottom oxide layer (col. 8, lines 55-60 and FIG. 33).

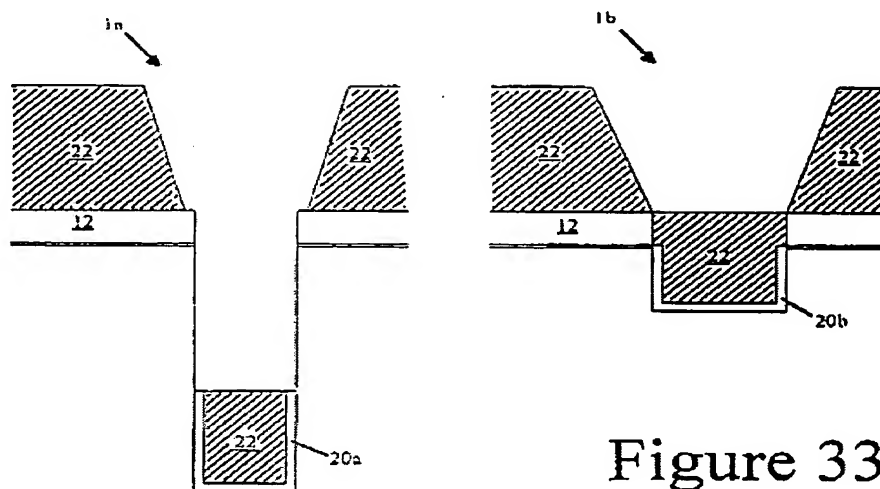


Figure 33

In re claim 2, Beintner discloses that the step (a) further comprises:

(a1) forming a pad oxide layer **11** on the semiconductor substrate **10**;

(a2) forming a silicon nitride layer **12** on said pad oxide layer **11** (col. 3, lines 50-61 and FIG. 1); and

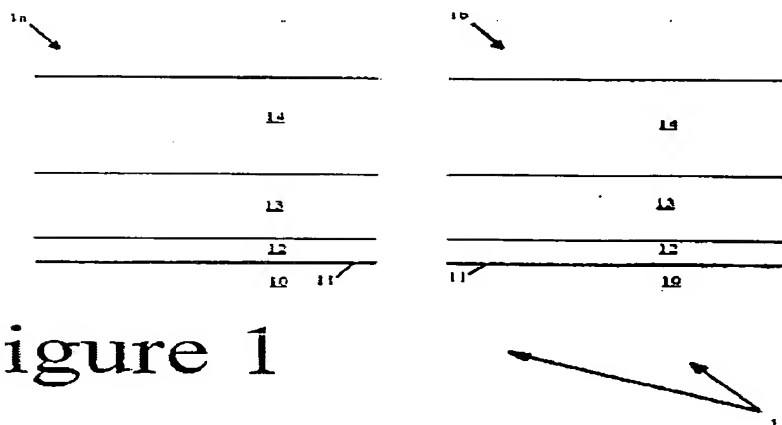


Figure 1

(a3) removing the silicon nitride layer 12, the pad oxide layer 11 and the semiconductor substrate 10 partially to form the trench structure 15a, 15b (col. 3, line 62 to col. 4, line 7 and FIG. 2).

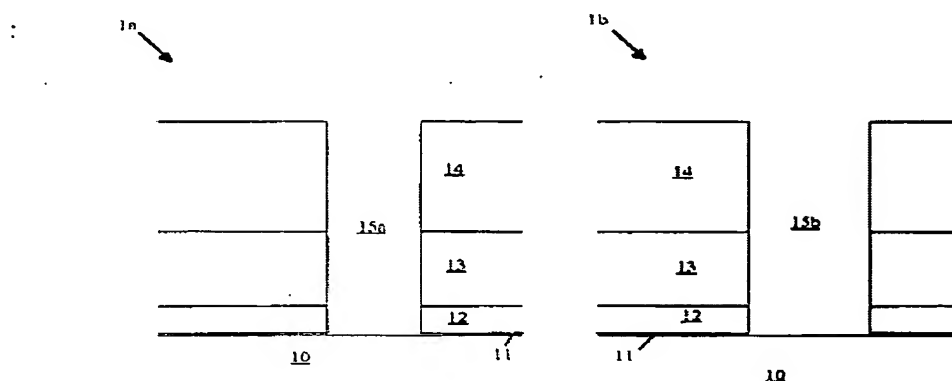


Figure 2

In re claim 3, Beintner discloses that the step (a3) is performed by a photolithography and dry-etching process (col. 3, lines 63-64).

In re claim 4, Beintner discloses that the trench structure has an aspect ratio between about 3.0 and about 4.0 (FIGS. 1-2).

In re claim 6, Beintner discloses that a ratio of a thickness of the oxide layer 22 deposited on the bottom of the trench structure 15a' to a thickness of the oxide layer deposited on the sidewall of the trench structure 15a' is between about 1.5 and about 2.3 (FIG. 32).

In re claim 7, Beintner discloses that the step (c) is performed by a wet-etching process (col. 8, lines 55-60).

In re claim 8, Beintner discloses that an etching selectivity of the oxide layer 22 on the sidewall of the trench structure 15' to the oxide layer 22 on the bottom of the trench structure is between about 2.5 and about 3 (FIG. 33).

In re claim 9, **Beintner** discloses that after the step (c), the steps of depositing and removing the oxide layer **22** are repeated in sequence for allowing the bottom oxide layer **22'** to reach a required thickness (col. 8, lines 54-60).

In re claim 10, **Beintner** discloses that the oxide layer **22** comprises a silicon oxide layer (col. 6, lines 31-39).

In re claim 11, **Beintner** discloses a method of fabricating a trench-type power MOSFET, the method comprising:

(a) providing a semiconductor substrate **10** and forming a trench structure **15a'** on the semiconductor substrate **10** (col. 7, lines 29-38 and FIG. 30);

(b) performing the plasma-enhanced chemical vapor deposition (PECVD) process without bias sputtering, with tetraethylorthosilicate (TEOS) as a gas source at a temperature of about 440°C to about 520°C to deposit an oxide layer **22** on the bottom and sidewall of the trench structure **15a'** and the semiconductor substrate **10**, the oxide layer **22** only partially filling the trench **15a'** (col. 8, lines 52-60 and FIG. 32); and

(c) removing, using a single etching process, the oxide layer **22** on the sidewall of the trench structure **15a'** substantially completely and the oxide layer **22** on the bottom of the trench structure partially to define the remaining oxide layer **22'** as the bottom oxide layer (col. 8, lines 55-60 and FIG. 33); and

(d) forming the trench-type power MOSFET device^e in the trench structure.

In re claim 12, **Beintner** discloses wherein the step (a) further comprises:

(a1) forming a pad oxide layer **11** on the semiconductor substrate **10**;

(a2) forming a silicon nitride layer 12 on the pad oxide layer 11 (col. 3, lines 50-61 and FIG. 1); and

(a3) removing the silicon nitride layer 12, the pad oxide layer 11 and the semiconductor substrate 10 partially to form the trench structure 15a, 15b (col. 3, line 62 to col. 4, line 7 and FIG. 2).

In re claim 13, Beintner discloses wherein the step (a3) is performed by a photolithography and dry-etching process (col. 3, lines 63-64).

In re claim 14, Beintner discloses that the trench structure has an aspect ratio between about 3.0 and about 4.0 (FIGS. 1-2).

In re claim 16, Beintner discloses that a ratio of a thickness of the oxide layer 22 deposited on the bottom of the trench structure 15a' to a thickness of the oxide layer 22 deposited on the sidewall of the trench structure 15a' is between about 1.5 and about 2.3 (FIG. 32).

In re claim 17, Beintner discloses that the step (c) is performed by a wet-etching process (col. 8, lines 55-60).

In re claim 18, Beintner discloses that an etching selectivity of the oxide layer 22 on the sidewall of the trench structure 15' to the oxide layer 22 on the bottom of the trench structure is between about 2.5 and about 3 (FIG. 33).

In re claim 19, Beintner discloses that between the steps of (c) and (d), the steps of depositing and removing the oxide layer 22 are repeated in sequence for allowing the bottom oxide layer 22' to reach a required thickness (col. 8, lines 54-60).

In re claim 20, Beintner discloses that the oxide layer **22** comprises a silicon oxide layer (col. 6, lines 31-39).

In re claim 21, Beintner discloses a method of forming a bottom oxide layer in a trench structure, the method comprising:

(a) providing a substrate **10** including a trench **15a'** having a bottom and a sidewall (col. 7, lines 29-38 and FIG. 30);

depositing an oxide layer **22** on the bottom and sidewall of the trench **15a'** by plasma-enhanced chemical vapor deposition (PECVD) process without bias sputtering with tetraethylorthosilicate (TEOS) as a gas source at a temperature of about 440°C to about 520°C, the oxide layer only partially filling the trench **15a'** (col. 8, lines 52-60 and FIG. 32); and

removing, using a single etching process, the oxide layer on the sidewall of the trench **15a'** substantially completely and the oxide layer **22** on the bottom of the trench partially to form a remaining oxide layer **22'** as the bottom oxide layer on the bottom of the trench (co. 8, lines 52-60 and FIG. 32).

In re claim 22, Beintner that the oxide layer **22** is removed by a wet-etching process having a higher etching selectivity of the oxide layer on the sidewall of the trench **15a'** to the oxide layer on the bottom of the trench (col. 8, lines 54-60).

In re claim 23, Beintner discloses that the etching selectivity of the oxide layer **22** on the sidewall of the trench **15a'** to the oxide layer **22** on the bottom of the trench is between about 2.5 and about 3 (FIG. 33).

In re claim 24, **Beintner** discloses that the deposited oxide layer 22 has a ratio of thickness on the bottom of the trench 15a' to thickness on the sidewall of the trench of higher than about 1.5 (col. 8, lines 54-60 and FIG. 33).

In re claim 25, **Beintner** discloses that the deposited oxide layer 22 has a ratio of thickness on the bottom of the trench 15a' to thickness on the sidewall of the trench of lower than about 2.3 (col. 8, lines 54-60 and FIG. 33).

In re claims 1, 5, 11, 15 and 21, **Beintner** does not explicitly disclose that the plasma-enhanced chemical vapor deposition (PECVD) process is performed at a temperature of about 440°C to about 520°C. However, there is no evidence indicating the temperature range is critical and it has been held that it is not inventive to discover the optimum or workable range of a result-effective variable within given prior art conditions by routine experimentation. See MPEP § 2144.05. Note that the specification contains no disclosure of either the critical nature of the claimed dimensions of any unexpected results arising there from. Where patentability is aid to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Response to Applicants' Amendment and Argument

Applicants contend that AAPA does not teach performing a plasma enhanced chemical vapor deposition (PECVD) process without bias sputtering with tetraethylorthosilicate (TEOS) as a gas source at a temperature of about 440°C to about 520°C to deposit an oxide layer on the bottom and sidewall of the trench structure and the

semiconductor substrate, the oxide layer only partially filling the trench; and removing, using a single etching process, the oxide layer on the sidewall of the trench structure substantially completely and the oxide on the bottom of the trench structure partially to define a remaining oxide layer as the bottom oxide layer.

In response to Applicants' contention that AAPA does not teach performing a plasma enhanced chemical vapor deposition (PECVD) process without bias sputtering with tetraethylorthosilicate (TEOS) as a gas source at a temperature of about 440°C to about 520°C to deposit an oxide layer on the bottom and sidewall of the trench structure and the semiconductor substrate, the oxide layer only partially filling the trench; and removing, using a single etching process, the oxide layer on the sidewall of the trench structure substantially completely and the oxide on the bottom of the trench structure partially to define a remaining oxide layer as the bottom oxide layer, Examiner respectfully disagrees. Applicants' argument is moot since the newly discovered reference, Beintner et al. (U.S. Patent 6,566,228) disclose Applicants' claimed invention (Applicants are directed to page 2, 1st paragraph to page 4, 2nd paragraph presented in this Office Action).

For this reason, Examiner holds the rejection proper.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khiem D. Nguyen whose telephone number is (571) 272-1865. The examiner can normally be reached on Monday-Friday (8:30 AM - 5:30 PM).

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (571) 272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

K.N.
April 09th, 2005



W. DAVID COLEMAN
PRIMARY EXAMINER